Supporting information for:

Graphene-Graphite Oxide Field-Effect Transistors

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Low Temperature Processing

Graphite oxide is known to decompose/reduce at temperatures as low as 100° C,[S1] which may impose a limit on the thermal processing steps needed to fabricate devices. In our case, the relevant step is the pre-baking performed after spinning on bilayer PMMA electron-beam resist. To further investigate this effect, we deposited graphite oxide flakes on several Si/SiO_2 substrates and then performed simulated e-beam lithography while varying the pre-baking temperature and time. Optical microscopy images of the flakes were recorded before and after using identical settings (illumination, aperture, exposure, gain, and color balance). The observed color was then used as a qualitative measure of the resistivity[S2,S3] and remaining oxidation of the partially-reduced flakes.

Images of a sample baked using a typical recipe: 170° C for 15 minutes are shown in Fig. S1. The graphite oxide flake changed color from blue-green to purple, indicating significant reduction.

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A subsequent test using 150° C for 25 minutes showed less color change, while another at 120° C for 25 minutes showed no color change at all. This suggests that 115° C for 15 minutes is a "safe" recipe when working with graphite oxide.

a b

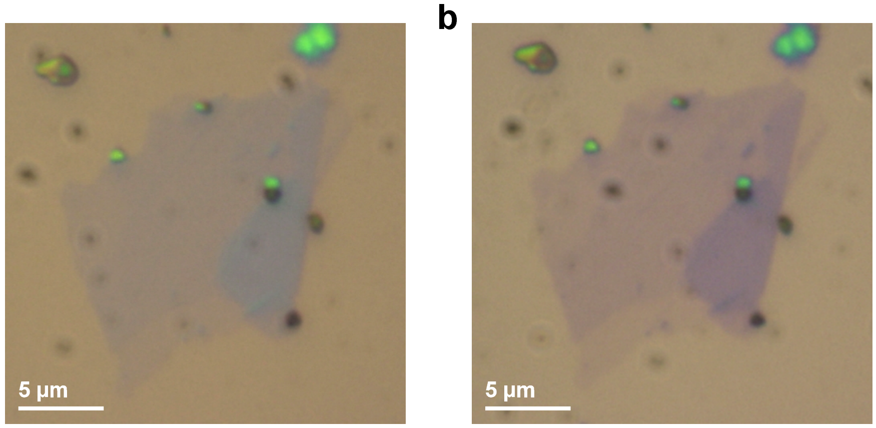

Figure S1: Optical microscopy image under white light of a graphite oxide flake (a) immediately after deposition and (b) after a simulated e-beam lithography process.

Another test was performed to determine whether the resolution of patterns created using the "safe" recipe would be significantly degraded. A 0.5 μm-scale test pattern was written at a range of electron doses and then metallized using thermal evaporation and liftoff. The best results were obtained when the dose was reduced approximately 10% (270 vs. 300 μC/cm^2 in our case) and were similar in quality to patterns made using the "standard" recipe.

Temperature Dependence of Leakage Current

The gate leakage current for devices processed using the "standard" recipe shows a strong dependence on temperature T. Gate conductance for two such devices plotted on a log scale against $T^{-1/4}$ is shown in Fig. S2. The linear decrease of $ln(G_{tg})$ down to 10 K is consistent with a variable-range hopping model.

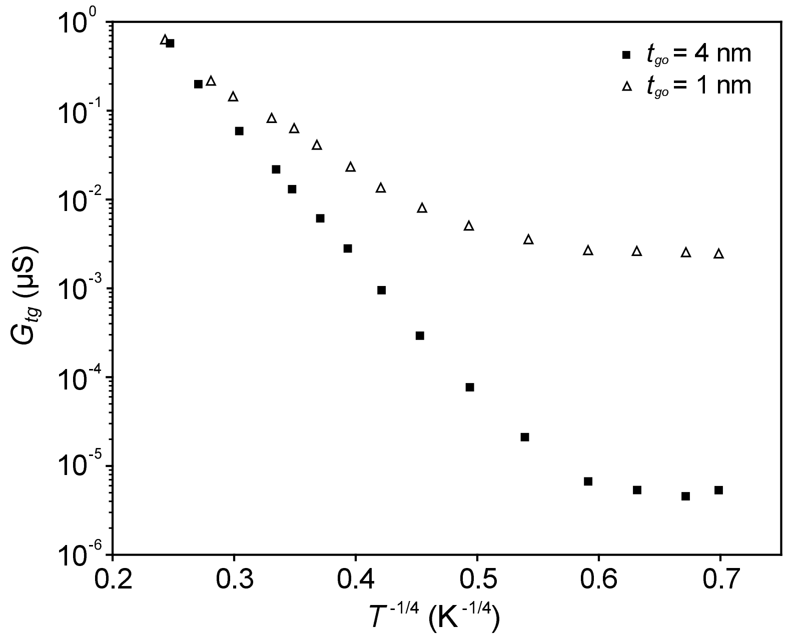

Figure S2: Gate conductance vs. temperature for two graphene-graphite oxide devices.

Summary of Devices and Their Breakdown Voltage

We fabricated approximately 10 devices using the high-temperature process and 20 devices using the low-temperature process. A significant fraction were found to have top-gate shorts, possibly caused by errors in lithography alignment or undetected pin-holes in the graphite oxide. Adopting a layer-transfer process to obtain more uniform graphite oxide or a self-aligned top-gate would likely improve the yield. We established safe top-gate voltage limits as part of measuring each fully functional transistor device, listed in Table S1. The actual breakdown electric field is likely to be slightly higher than the values below.

Table S1: Maximum applied gate stress for several G-GO transistors.

t_{go} (nm)	V_{max} (V)	E_{max} (V/m)
4	1.3	3.1×10^{8}
$\sim$10	1.0	1.0×10^{8}
18	4.2	2.3×10^{8}
35	3.5	1.0×10^{8}

References

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